What is claimed is:

1. A semiconductor device comprising a non - volatile memory, said non - volatile memory including:

a memory cell array constituted by memory cells which have floating electrodes and are arranged in the shape of a matrix on a semiconductor substrate;

element isolating regions, each of which has a first trench formed in said semiconductor substrate and between said memory cells adjacent to each other along a gate width direction, and an isolating filler filled in said first trench;

a second trench formed in said isolating filler and between said floating electrodes of said memory cells adjacent to each other along the gate width direction and being narrow at the bottom thereof; and

a word line connected to said memory cells, buried in said second trenches and extending along the gate width direction.

2. The semiconductor device of claim 1, wherein said second trench is capable of reducing parasitic capacitance between said floating electrodes of said memory cells adjacent to each other along the gate width direction.

3. The semiconductor device of claim 1, wherein said second trench is in the shape of V.

4. The semiconductor device of claim 1, wherein said second trench is in the shape of an inverted trapezoid.

5. The semiconductor device of claim 1, wherein said second trench is in the shape of U.

6. The semiconductor device of claim 1, wherein each of said memory cells includes a control electrode with a gate insulating film provided on said floating electrode, and said word line is made of a material same as that of said control electrode, is integral with and on the same conductive layer with said control electrode.

7. The semiconductor device of claim 6, wherein said word line is buried in said second trench via an insulating film, said insulating film and said gate insulating film being on the same insulating layer.

8. The semiconductor device of claim 1, wherein said gate insulating film includes at least a silicon nitride film.

9. The semiconductor device of claim 1, wherein a ratio of a top diameter to a bottom diameter of said second trench is large compared with a ratio of those of said first trench.

10. The semiconductor device of claim 1, wherein said second trench is shallower than said first trench and extends below a surface of said semiconductor substrate.

11. The semiconductor device of claim 1, wherein said non - volatile memory is a NAND or NOR type electrically erasable programmable read only memory.

12. A method of manufacturing a semiconductor device including a non - volatile memory, the method comprising:

making an element isolating region by forming a first trench in a semiconductor substrate between memory cell forming regions adjacent to each other along a gate width direction, and by filling said first trench with an isolating filler;

making a floating gate electrode on said semiconductor substrate at said memory cell forming regions, said floating gate electrode having a predetermined gate width;

making a second trench in said isolating filler filled in said first trench and between floating electrodes adjacent to each other along a gate width direction, said second trench being narrow at bottoms thereof; and

forming a word line in said second trench, said word line extending along the gate width direction.

13. The method of claim 12, wherein said second trench is formed in the shape of V.

14. The method of claim 12, wherein said second trench is formed in the shape of an inverted trapezoid.

15. The method of claim 12, wherein said second trench is formed in the shape of U.

16. The method of claim 12, wherein said second trench is in self - alignment to said floating electrodes.

17. A method of manufacturing a semiconductor device including a non - volatile memory, the method comprising:

making floating gate electrodes on a semiconductor substrate at memory cell forming regions, said floating gate electrode having a predetermined gate width;

making a first trench in said semiconductor substrate and between said floating gate electrodes adjacent to each other along a gate width direction, said first trench being in self - alignment to said floating gate electrode;

making an element isolating region by filling an isolating filler in said first trench;

making a side wall spacer on a surface of said isolating filler in a side wall of said floating gate electrodes, said side wall spacer being in self - alignment to said floating gate electrodes;

making a second trench in said isolating filler filled in said first trench using said side wall spacer as a mask; and

forming a word line in said second trench, said word line extending along the gate width direction.